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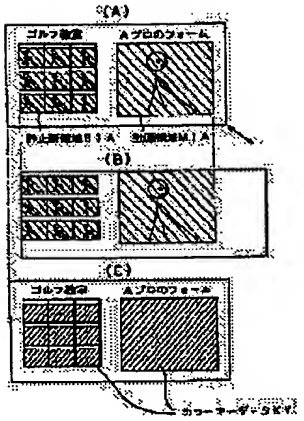
(54) IMAGE DISPLAY METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To display a stationary image and a moving image simultaneously while scaling.

SOLUTION: A still image signal is written in a still image area SIA in an image memory 310. A moving image signal is written in a moving image area MIA in the image memory 310, the image is scaled while the image signal written in the image memory 310 is read, and the image signal after the scaling is supplied to a display device. As a result, the dynamic image and the still image scaled simultaneously are displayed on the display device.



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CLAIMS

[Claim(s)]
[Claim 1] The process which is the approach of displaying an animation and a still picture on the display device of a computer system at coincidence, and writes (a) still picture video signal in the still picture field in image memory, (b) While writing an animation video signal in the animation field in said image memory The graphic display approach equipped with the process which displays the animation by which the scaling was carried out by performing the scaling of an image, reading the video signal currently written in said image memory, and supplying the video signal after a scaling to a display device, and a still picture on a display device.
[Claim 2] It is the approach of displaying an animation and a still picture on the display device of a computer system at coincidence. (a) The process which writes in the key data in which a superimposition field is shown in the 1st image memory which has the room corresponding to the display screen of a display device, (b) The process which writes a still picture video signal in the still picture field in the 2nd image memory, (c) Writing an animation video signal in the animation field in said 2nd image memory continuously By performing the scaling of the process which reads the 1st video signal currently written in said 2nd image memory, and the image expressed with the 1st video signal of (d) above By compounding said 2nd video signal in said superimposition field of the image expressed with the process which searches for the 2nd video signal, and the 3rd video signal read from the image memory of the (e) above 1st The graphic display approach equipped with the process which searches for the 4th video signal, and the process which displays the animation by which the scaling was carried out by supplying the 4th video signal of (f) above to a display device, and a still picture on a display device.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the approach of displaying an animation and a still picture on the display device of a computer system at coincidence.

[0002]
[Description of the Prior Art] Drawing 12 is the explanatory view showing the condition that the still picture and the animation were displayed by coincidence in one window of a display device. In order to realize such a display, the still picture and the animation are conventionally memorized to another video memory, and the overlay technique compounded in the case of a display is used.
[0003] By the way, it is possible to change the size of each window in multi-window systems, such as MS-WINDOWS (trademark of Microsoft Corp.). In case the size of a window is changed, the approach of making large the range of the image displayed in a window, without changing the scale factor of an image and the display rectangle of an image have the approach of carrying out the scaling of the image, without changing.
[0004]
[Problem(s) to be Solved by the Invention] However, it was difficult to express as the conventional overlay technique on the occasion of modification of the size of a window, carrying out the scaling of a still picture and the animation to coincidence.
[0005] This invention is made in order to solve the above-mentioned technical problem in the conventional technique, and it aims at what is displayed carrying out the scaling of a still picture and the animation to coincidence.
[0006]
[The means for solving a technical problem, and its operation and effectiveness] In order to solve a part of above-mentioned technical problem [at least], the 1st invention The process which is the approach of displaying an animation and a still picture on the display device of a computer system at coincidence, and writes (a) still picture video signal in the still picture field in image memory, (b) While writing an animation video signal in the animation field in said image memory It has the process which displays the animation by which the scaling was carried out, and a still picture on a display device by performing the scaling of an image, reading the video signal currently written in said image memory, and supplying the video signal after a scaling to a display device.
[0007] A still picture and an animation are written in in image memory, and since the scaling of an image is performed reading the video signal showing the image containing these, the scaling of a still picture and the animation is carried out to coincidence. And since the video signal after a scaling is supplied to a display device, the still picture and animation by which the scaling was carried out to coincidence can be displayed on a display device.
[0008] The 2nd invention is the approach of displaying an animation and a still picture on the display device of a computer system at coincidence. (a) The process which writes in the key data in which a superimposition field is shown in the 1st image memory which has the room corresponding to the display screen of a display device, (b) The process which writes a still picture video signal in the still picture field in the 2nd image memory, (c) Writing an animation video signal in the animation field in said 2nd image memory continuously By performing the scaling of the process which reads the 1st video signal currently written in said 2nd image memory, and the image expressed with the 1st video signal of (d) above By compounding said 2nd video signal in said superimposition field of the image expressed with the process which searches for the 2nd video signal, and the 3rd video signal read from the image memory of the (e) above 1st It has the process which searches for the 4th video signal, and the process which displays the animation by which the scaling was carried out by supplying the 4th video signal of (f) above to a display device, and a still picture on a display device.
[0009] A still picture and an animation are written in the 2nd image memory, and since the scaling of an image is performed reading the 1st video signal showing the image containing these, the 2nd video signal with which a still picture and an animation express the image by which the scaling was carried out to coincidence is acquired. This 2nd video signal is compounded in the superimposition field of the 3rd video signal read from the 1st image memory. Therefore, it can insert in in the superimposition field of a display device, carrying out the scaling of a still picture and the animation to coincidence.

[0010]
[Other modes of invention] This invention contains other following modes. the 1st mode — the 2nd invention — setting — further — (g) — while changing the scale factor of the scaling in said process (d), it has the process which changes said key data remembered to carry out the scaling of said superimposition field for said scale factor by said 1st image memory.
[0011] Since the scaling of the superimposition field will be carried out for the same scale factor even if it changes the scale factor of the scaling of a still picture and an animation if it carries out like this, a part for the display of a still picture and an animation is kept the same as scaling before.
[0012]
[Embodiment of the Invention]
A. Explain the gestalt of whole equipment configuration:, next operation of this invention based on an example. Drawing 1 is the block diagram showing the configuration of the computer system which applies one example of this invention. As for this computer system, CPU620, main memory 630, the circumference controller 640, compound I / 0 port 650, a network interface 656, a video controller 660, 1st Video RAM (VRAM) 670, the image transfer controller 680, and the image processing circuit 800 are connected to the bus 610. The image processing circuit 800 has 2nd Video RAM 310 in the interior. In addition, 1st VRAM670 has the viewing area of a color CRT 701, and the memory area corresponding to 1 to 1.
[0013] The keyboard 642 and the mouse 644 are connected to the circumference controller 640. Moreover, the floppy disk drive unit 652 and the hard disk drive unit 654 are connected to compound I/O Port 650.
[0014] The color CRT 701 (or color liquid crystal display) as a display device is connected to the video controller 660. A video controller 660 has the function which reads a video signal from 1st VRAM670, and is supplied to the image processing circuit 800 while writing the image data of a still picture in 1st VRAM670. Further, a video controller 660 generates a synchronizing signal SYNC (Vertical Synchronizing signal VSPC and Horizontal Synchronizing signal HSPC), and has the function supplied to a color CRT 701 and the image processing circuit 800.
[0015] The CD-ROM equipment 682 as an animation image data feeder is connected to the image transfer controller 680. The image transfer controller 680 has the function as a processor which transmits the animation image data given from CD-ROM equipment 682 to 2nd VRAM310 through a bus 610.
[0016] The image processing circuit 800 has the function which supplies the video signal showing the image after composition to a color CRT 701 while compounding an animation video signal and a still picture video signal. Moreover, the image processing circuit 800 has the function which carries out zooming of a still picture and the animation to coincidence by carrying out the scaling of the video signal after composition.
[0017] B. The internal configuration of the image processing circuit 800 : drawing 2 is the block diagram showing the internal configuration of the image processing circuit 800. In addition, the configuration of this image processing circuit 800 is the same as that of what is indicated in Fig. 4 of JP,2-298176,A indicated by these people.
[0018] This image processing circuit 800 has the voice section ACU which deals with a sound signal, the analog section ANU which deals with analog video signals, such as a TV signal, the image memory section IMU, the write control section WCU which controls the writing of the image data to the image memory section IMU, the read-out control section RCU which reads outside the image data memorized by the image memory section IMU, and the image reproduction section IRU which reproduces an image.
[0019] The voice section ACU has the voice input terminal 101, the sound signal selection circuitry 110, the sound-volume control circuit 120, and the voice output terminal 102. The sound signal ASEX given from animation signal feeders, such as a video player, is inputted into the voice input terminal 101. The sound signal selection circuitry 110 chooses and outputs one side of this sound signal ASEX and the

sound signal ASTV inputted from the television tuner 710 of the analog section ANU. In addition, the channel selection in the television tuner 710 is directed from CPU620. Sound volume is adjusted by the sound-volume control circuit 120, and the selected sound signal is outputted from the voice output terminal 102. The sound signal ASMON outputted from the voice output terminal 102 is given to the voice input terminal or loudspeaker of a color CRT 701.

[0020] The analog section ANU has the television tuner 710, TV antenna 711, the image input terminal 103, the video-signal selection circuitry 130, the video-signal decoder 140, A-D converter 210, and the digitization control circuit 220. The video signal VSEX given from the animation signal feeder is inputted into the image input terminal 103. The video-signal selection circuitry 130 chooses and outputs one side with the video signal VSTV given from the television tuner 710 by which channel selection directions were carried out with these video signals CPU [VSEX and] 620. The selected video signal is divided into a video signal LSTV and a synchronizing signal SSTV by the video-signal decoder 140. This video signal LSTV is a chrominance signal of RGB in three primary colors. A-D converter 210 changes into a digital signal the video signal LSTV which is an analog signal, and supplies it to the write control section WCU. The digitization control circuit 220 is controlling A-D converter 210 based on a synchronizing signal SSTV, and is controlling VRAM310 via the write control section WCU.

[0021] The write control section WCU has the image data selection circuitry 320, the image memory control signal selection circuitry 330, and the write control circuit 340. The image data selection circuitry 320 chooses and outputs one side of the output of A-D converter 210 which considers a video signal LSTV as an input, and the video signal LSWPC read from external devices, such as external storage, by CPU620 according to the write-in selection signal CC outputted from the write control circuit 340. The image memory control signal selection circuitry 330 chooses and outputs one side of the image memory control signal WETV which the digitization control circuit 220 outputs, and the image memory control signal WEPC which the write control circuit 340 outputs according to the write-in selection signal CC. The write control circuit 340 controls the actuation which writes the video signal LSWPC supplied from CPU620 or the image transfer controller 680 in the image memory section IMU.

[0022] The read-out control section RCU has the read-out control circuit 350, FIFO memory (FIFO memory) 360, and the FIFO read-out control circuit 370. The video signal LSFIF read from the image memory section IMU by the FIFO read-out control circuit 370 is memorized by FIFO memory 360. The video signal LSFIF memorized by FIFO memory 360 is read outside by the read-out control circuit 350. The read-out control section RCU is used in case the image data memorized by the image memory section IMU are outputted to an external device according to the instruction of CPU620.

[0023] The image memory section IMU has the 3 port VRAM 310 which has one write-in port and two read-out ports. As 3 port VRAM 310, CXK1206 by Sony Corp. or MB81C1501 by FUJITSU, LTD. can be used. About the configuration and function of the 3 port VRAM 310, since it is indicated by JP,2-298176,A indicated by these people, explanation is omitted here. In addition, especially this VRAM310 should just be memory which does not restrict to three ports and memorizes image data.

[0024] The image reproduction section IRU compounds the video signal LSMEM outputted from the video signals VRAM [LSPC and] 310 outputted from the video controller 660, generates the synthetic video signal LSMON, and has the function which outputs this to a color CRT 701.

[0025] Each signal in the image reproduction section IRU expresses the following contents, respectively.

LSPC: The video signal outputted from the video controller 660.

The video signal read from LSMEM:VRAM310.

LSDA: The analog-ized video signal.

LSMON: The synthetic video signal showing the image displayed on a color monitor 701.

[0026] CNT: The change-over signal which switches the video switch 510. When the change-over signal CNT is H level, a video signal LSDA is chosen, and when it is L level, a video signal LSPC is chosen.

[0027] SENBL: The 1st enabling signal which specifies the propriety of a superimposition. The 1st enabling signal SENBL will switch to H level, if an operator specifies the mode which superimposes using

a keyboard 642 or a mouse 644, and if the mode which does not superimpose is specified, it will switch to L level.
SSENBL: The 2nd enabling signal which shows the timing equivalent to the superimposition field on a screen. The 2nd enabling signal SSENBL serves as H level in a Spa imposing field, and serves as L level out of a superimposition field. In addition, a superimposition field is specified by the operator on the screen of a color monitor 701.
NENBL: The 3rd enabling signal which shows the propriety of a multiplex superimposition. It is shown whether the 3rd enabling signal NENBL superimposes a video signal LSPC further to a part of video signal LSDA superimposed to the video signal LSPC.
[0028] COMP: The signal which shows the field of a multiplex super superimposition. The level of this comparison signal COMP is determined by comparing a video signal LSPC with the predetermined reference voltage Vr, and turns into H level in the field which superimposes a video signal LSPC to a part of video signal LSDA. The comparison signal COMP is confirmed when the enabling signal CENBL described below is H level, and it turns into the 3rd above-mentioned enabling signal NENBL.
CENBL: The enabling signal which specifies the propriety of a multiplex superimposition. The level of an enabling signal CENBL is switched by the operator.
[0029] DA converter 410 in the image reproduction section IRU changes into an analog signal the video signal LSMEM read from VRAM310, and supplies it to the video switch 510. The video switch 510 chooses one side of the video signal LSPC outputted from the video controller 660, and the video signal LSDA outputted from DA converter 410, and supplies it to a color CRT 701 as a synthetic video signal LSMON. The selection signal CNT of the video switch 510 is an output signal of AND circuit 451.
[0030] The superimposition control circuit 420 has the function which carries out the scaling of the image expressed with the video signal while reading the video signal memorized by VRAM310 in the image processing circuit 800.
[0031] B. — the detail configuration of the superimposition control circuit 420, and : of operation — drawing 3 is the block circuit diagram of the superimposition control circuit 420 and its circumference circuit. Moreover, as for the 3 port VRAM 310 shown here, a read-out port is used among three input/output port. The timing chart concerning the above-mentioned read-out port is indicated by 27th page – the 31st page of data sheet number 71215-ST of CXK1206 by Sony Corp. The port to be used is the lead port 1 of the 2nd page of the above-mentioned data sheet.
[0032] the 3 port VRAM 310 — memory drive clock signal HDCK — the port 1 shift signal terminal CKR1 — a memory perpendicular / level reset-signal MRST — the port 1 perpendicular clear terminal VCLR1 — the perpendicular offset signal VROFT or perpendicular read-out Rhine clock signal VRLCK is given to the port increment terminal INC1 of one line, and port 1 output enabling [RE1 (negative logic)] is given to the port 1 level clear terminal HCLR1 for horizontal reset-signal HRST at the port 1 output enabling terminal RE1 (negative logic), respectively. Moreover, the analog RGB signal LSMEM (one data in R, G, and B respectively) is read from the port 1 data output DO10-DO13.
[0033] To every R, G, and B, the analog RGB signal LSMEM by which read-out control is carried out is 4 bits, and is outputted by the port 1 shift signal CKR1 corresponding to each above-mentioned terminal, port 1 perpendicular clear VCLR1, the port 1 level clear signal HCLR1, the port increment signal INC1 of one line, and port 1 output enabling [RE1 (negative logic)] from the port 1 data output DO10-DO13, respectively.
[0034] The video switch 510 outputs the input of a generator terminal or a battery terminal from the common terminal C with the change-over signal VSEL inputted into the change-over signal input terminal CNT. When the change-over signal VSEL is high level "H", the input of a battery terminal is specifically outputted, and the input of a generator terminal is outputted from C terminal, respectively at the time of a low level "L." CPU620 controls each part through the bus 610 in a personal computer.
[0035] 421 of drawing 3 shows the level criteria read-out dot clock generator which outputs the level criteria read-out dot clock signal HBDCK, 422 shows the level read-out initiation counter which outputs

the horizontal read-out start signal HRSA and horizontal read-out direction reset-signal HRST, 423 shows the level 64 clock counter which outputs a level criteria start signal HRSB, 424 shows the count counter of level read-out which outputs the count signal HRT of horizontal read-out, and 425 shows the level read-out dot clock generator which outputs a horizontal read-out dot clock signal HDDA. Moreover, the perpendicular read-out offset counter 426 is the number of counts which synchronized with the level criteria read-out dot clock generator 421, and outputs the perpendicular read-out offset signal VROFT which determines the offset line of read-out Rhine of the perpendicular direction of the 3 port VRAM 310. The number counter 427 of perpendicular blankings outputs the perpendicular blanking terminate signal VBE, the perpendicular read-out initiation counter 428 outputs the perpendicular read-out start signal VRS, the count counter 429 of perpendicular read-out outputs the count signal VRT of perpendicular read-out, and the perpendicular read-out Rhine clock generation machine 430 outputs perpendicular read-out Rhine clock signal VRLCK. AND circuit 431 outputs the change-over signal VSEL which makes two video signals LSPC and LSDA superimpose, OR circuit 432 outputs the perpendicular read-out offset signal VROFT and perpendicular read-out Rhine clock signal VRLCK as a port increment signal INC1 of one line, and NOR circuit 433 outputs lead enabling RE1 signal. Moreover, signs 434 and 435 show a tri-state circuit, and 436 shows an inverter circuit.

[0036] The chrominance signal of the video signal LSPC which comes from the chrominance-signal input terminal 506 is given to the generator terminal of the video switch 510. Horizontal Synchronizing signal HSPC which comes from the synchronous terminal 507 which constitutes the Horizontal Synchronizing signal of an input terminal 506 The level criteria read-out dot clock generator 421, the horizontal read-out initiation counter 422, the horizontal 64 clock counter 423, the count counter 424 of horizontal read-out, the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428, the count counter 429 of perpendicular read-out, While the perpendicular read-out Rhine clock generation machine 430 is given, Vertical Synchronizing signal VSPC The 3 port VRAM 310, the perpendicular read-out offset counter 426, the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428, the count counter 429 of perpendicular read-out, and the perpendicular read-out Rhine clock generation machine 430 are given. Moreover, synchronizing signals HSPC and VSPC are sent out also to the synchronizing signal terminals 490 and 491, respectively.

[0037] Here, I/O of Horizontal Synchronizing signal HSPC and Vertical Synchronizing signal VSPC is explained using drawing 4 . Horizontal Synchronizing signal HSPC and Vertical Synchronizing signal VSPC are given in the necessary circuit shown in drawing 3 in the synchronizing signal terminal 490,491 and the superimposition control circuit 420 through buffers 62 and 61. These buffers 61 and 62 are contributed to exact transmission of the above-mentioned synchronizing signal, even when it has functions, such as IMPI Dines conversion and waveform shaping, and cascade connection of the image processing system is carried out. Moreover, Horizontal Synchronizing signal HSPC is given in the PLL circuit 63 in the level criteria read-out dot clock generator 421, and the level criteria read-out dot clock HBDCK is generated as a signal which specifies the horizontal resolution of the whole water horizontal plane specified by CPU620.

[0038] The PLL circuit 63 is constituted as shown in drawing 5 . That is, Horizontal Synchronizing signal HSPC is given from a signal line 70 to a phase comparator 71, and the output of the N counting-down circuit 74 is given to a phase comparator 71, in a phase comparator 71, the phase comparison of these signals is performed and the signal of the pulse width corresponding to phase contrast is outputted. The output of a phase comparator 71 is given and graduated by the low pass filter 72, and is given to a voltage controlled oscillator (VCO) 73. It oscillates on the frequency according to the electrical potential difference given, and VCO73 is given to the N counting-down circuit 74, and dividing is carried out even to the frequency of Horizontal Synchronizing signal HSPC, and it is returned to a phase comparator 71 while it is sent out in each part, this being used as the level criteria read-out dot clock HBDCK. Consequently, the level criteria read-out dot clock HBDCK which synchronized with Horizontal Synchronizing signal HSPC is created.

[0039] As for the horizontal read-out initiation counter 422 in the superimposition control circuit 420 of drawing 3 , the level 64 clock counter 423, and the count counter 424 of horizontal read-out, the counted value is reset by Horizontal Synchronizing signal HSPC, respectively. Furthermore, Vertical Synchronizing signal VSPC which comes from the synchronous terminal 508 is sent out to port 1 perpendicular clear VCLR1, NOR circuit 433, the perpendicular read-out offset counter 426, the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428, the count counter 429 of perpendicular read-out, the perpendicular read-out Rhine clock generation machine 430, and the synchronizing signal terminal 491 of the 3 port VRAM 310, respectively. Moreover, as for the perpendicular read-out offset counter 426, the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428, and the count counter 429 of perpendicular read-out, the counted value is reset by Vertical Synchronizing signal VSPC, respectively.
[0040] The level criteria read-out dot clock signal HBDCK generated from the level criteria read-out dot clock generator 421 is sent out to the port 1 shift signal terminal CKR1 of the 3 port VRAM 310 as clock signal HDCK of the 3 port VRAM 310 through the tri-state circuit 435 while it is given to the horizontal read-out initiation counter 422, the horizontal 64 clock counter 423, the count counter 424 of horizontal read-out, and the perpendicular read-out offset counter 426.
[0041] Moreover, the horizontal read-out dot clock generator 425 is N1 of the frequency of Horizontal Synchronizing signal HSPC on the basis of the horizontal read-out reference signal HRSB from the horizontal 64 clock counter 423. It is constituted by the PLL circuit which outputs the signal of a twice as many frequency as this, and the horizontal read-out dot clock signal HDDA is outputted. The horizontal read-out dot clock signal HDDA generated by this horizontal read-out dot clock generator 425 is given as clock signal HDCK of the 3 port VRAM 310 through the tri-state circuit 434 to the port 1 shift signal terminal CKR1 and D-A converter 410 of the 3 port VRAM 310, and is used as the read-out clock signal of digital RGB code LSMEM, and a conversion clock signal of D-A converter 410.
[0042] Drawing 6 is the explanatory view showing the function of the set point of each circuit in the superimposition control circuit 420. As shown in drawing 6 , it is the frequency fHBDCK of the level criteria read-out dot clock signal HBDCK. The ratio (fHBDCK/fHDDA) of the frequency fHDDA of the horizontal read-out dot clock signal HRDCK is equal to the horizontal scale factor KH of the image (drawing 6 (A)) read from VRAM310, and the image (drawing 6 (B)) displayed on a color CRT 701. Therefore, it is possible by adjusting the frequency fHDDA of the horizontal read-out dot clock signal HDDA to expand horizontally the image displayed on a color CRT 701, or to reduce. If it puts in another way, it will be the dividing value N425 of the PLL circuit in the horizontal read-out dot clock generator 425. By adjusting a value, the scaling of the image can be carried out horizontally.
[0043] The perpendicular read-out Rhine clock generation machine 430 synchronizes with Vertical Synchronizing signal VSPC, and is N2 of the frequency of Vertical Synchronizing signal VSPC. It is constituted by the PLL circuit which outputs the signal of a twice as many frequency as this, and perpendicular read-out Rhine clock signal VRLCK is outputted. Perpendicular read-out Rhine clock signal VRLCK generated by this perpendicular read-out Rhine clock generation machine 430 is given through OR circuit 432 and NOR circuit 433 to port 1 output enabling RE1 terminal (negative logic) while it is given to the port increment terminal INC1 of one line which advances the Rhine address which is the address of the perpendicular direction of the 3 port VRAM 310 through OR circuit 432.
[0044] As shown in drawing 6 , it is the frequency fHSYNC of Horizontal Synchronizing signal HSPC. Frequency fVRLCK of perpendicular read-out Rhine clock signal VRLCK A ratio (fHSYNC/fVRLCK) is equal to the scale factor KV of the perpendicular direction of the image (drawing 6 (A)) read from the 3 port VRAM 310, and the image (drawing 6 (B)) displayed on a color CRT 701. Therefore, frequency fVRLCK of perpendicular read-out Rhine clock signal VRLCK By adjusting, it is possible to carry out zooming of the image displayed on a color CRT 701 perpendicularly. If it puts in another way, it will be the dividing value N430 of the PLL circuit in the perpendicular read-out Rhine clock generation machine 430. By adjusting a value, the scaling of the image can be carried out perpendicularly.

[0045] The superimposition control circuit 420 has obtained fundamental read-out timing by these level criteria read-out dot clock signal HBDCK, the horizontal read-out dot clock signal HDDA, and perpendicular read-out Rhine clock signal VRLCK.
[0046] The perpendicular read-out offset counter 426 sends out the perpendicular offset signal VROFT which carries out stepping of the Rhine address of the perpendicular direction of the 3 port VRAM 310 to OR circuit 432, synchronizing with the level criteria read-out dot clock signal HBDCK outputted from the level criteria read-out dot clock generator 421, after counted value is reset by Vertical Synchronizing signal VSPC, in order to decide the initiation offset-line location of read-out Rhine of the 3 port VRAM 310.
[0047] As shown in drawing 6 (A), the set point N426 of the perpendicular read-out offset counter 426 shows the starting position of the perpendicular direction of the image part (field enclosed with a drawing destructive line) read from the 3 port VRAM 310.
[0048] The number counter 427 of perpendicular blankings contains the counter (not shown) for making the perpendicular back porch field of a video signal LSPC delete. If this counter counts the number of clocks of Horizontal Synchronizing signal HSPC and a perpendicular back porch field is passed, it will output the perpendicular blanking terminate signal VBE to the perpendicular read-out initiation counter 428.
[0049] In response to the enabling signal (perpendicular blanking terminate signal VBE) sent out from the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428 counts the number of clocks of Horizontal Synchronizing signal HSPC, and outputs the read-out initiation enabling signal (perpendicular read-out start signal) VRS over the perpendicular direction from the 3 port VRAM 310 to the count counter 429 of perpendicular read-out.
[0050] As shown in drawing 6 (C), it is the set point N428 of the perpendicular read-out initiation counter 428. The vertical display starting position at the time of the image read from the 3 port VRAM 310 being displayed on the screen of a color CRT 701 is specified.
[0051] In response to the enabling signal (control signal VRS) sent out from the perpendicular read-out initiation counter 428, the count counter 429 of perpendicular read-out counts the number of clocks of Horizontal Synchronizing signal HSPC, and outputs the signal VRT which shows the read-out period over the perpendicular direction from the 3 port VRAM 310, i.e., the count signal of perpendicular read-out, to AND circuit 431.
[0052] As shown in drawing 6 (B) and (C), it is the set point N429 of the count counter 429 of perpendicular read-out. The number of Rhine of the perpendicular direction of the image displayed on a color CRT 701 is specified.
[0053] Read-out control of the perpendicular direction to the 3 port VRAM 310 is performed by the perpendicular read-out offset counter 426 explained above, the number counter 427 of perpendicular blankings, the perpendicular read-out initiation counter 428, the count counter 429 of perpendicular read-out, and the perpendicular read-out Rhine clock generation machine 430.
[0054] In addition, N426 clocks of the level criteria read-out dot clock signal HBDCK which the perpendicular read-out offset counter 426 counts, N427 clocks of Horizontal Synchronizing signal HSPC which the number counter 427 of perpendicular blankings counts, N428 clocks of Horizontal Synchronizing signal HSPC which the perpendicular read-out initiation counter 428 counts, The value of N counting-down circuit in the PLL circuit in clock several N 429 and perpendicular read-out Rhine clock generation machine 430 of Horizontal Synchronizing signal HSPC which the count counter 429 of perpendicular read-out counts is set as a necessary value by CPU620 in a personal computer, respectively.
[0055] The horizontal read-out initiation counter 422 counts the number of clocks of the level criteria read-out dot clock signal HBDCK sent out from the level criteria read-out dot clock generator 421, and sends out the read-out initiation enabling signal (horizontal read-out start signal HRSA) over the horizontal direction of the 3 port VRAM 310 to the horizontal 64 clock counter 423.

[0056] As shown in drawing 6 (C), it is the set point N422 of the horizontal read-out initiation counter 422. The horizontal display starting position at the time of the image read from the 3 port VRAM 310 being displayed on the screen of a color CRT 701 is specified.
[0057] The horizontal 64 clock counter 423 counts the number of clocks of the level criteria read-out dot clock signal HBDCK outputted from the level criteria read-out dot clock generator 421 in response to the enabling signal (horizontal read-out start signal HRSA) sent out from the horizontal read-out initiation counter 422. And if the counted value becomes 64 clocks which are the properties at the time of read-out of the 3 port VRAM 310, the horizontal read-out reference signal HRSB will be outputted to the horizontal read-out dot clock generator 425, the count counter 424 of horizontal read-out, and AND circuit 431.
[0058] The count counter 424 of horizontal read-out counts the number of clocks of the level criteria read-out dot clock signal HBDCK sent out from the level criteria read-out dot clock generator 421, and sends out the enabling signal (count signal HRT of horizontal read-out) of the read-out period over the horizontal direction of the 3 port VRAM 310 to AND circuit 431.
[0059] As shown in drawing 6 (B) and (C), it is the set point N424 of the count counter 424 of horizontal read-out. The horizontal number of dots of the image displayed on a color CRT 701 is specified.
[0060] In this way, horizontal read-out control to the 3 port VRAM 310 is performed by the horizontal read-out initiation counter 422, the horizontal 64 clock counter 423, and the count counter 424 of horizontal read-out. In addition, N422 clocks of the level criteria read-out dot clock signal HBDCK which the horizontal read-out initiation counter 422 counts among the set point of the counting-down circuit in the PLL circuit of the level criteria read-out dot clock generator 421, and the set point of the counting-down circuit in the PLL circuit of the horizontal read-out dot clock generator 425 N424 clocks of the criteria dot clock signal HBDCK which the count counter 424 of horizontal read-out counts It is set as a necessary value by CPU620 in a personal computer, respectively.
[0061] C. The contents of the image processing in the 1st example : drawing 7 is the explanatory view showing the contents of processing of the 1st example of this invention, and drawing 8 is a flow chart which shows the procedure. In addition, processing of drawing 8 is performed when CPU620 performs the application program stored in main memory 630.
[0062] In processing of the 1st example, as shown in drawing 7 (A), nine different professional golfers' photograph is displayed on the left half in one window of a color CRT 701 as a still picture. And the animation in which the professional golfer's golf swing jazz is shown is displayed on the right half of a window in which a user chooses one professional golfer using a mouse 644.
[0063] At step S1 of drawing 8 , CPU620 or the image transfer controller 680 reads the image data of a still picture from the CD-ROM equipment 682 which is external storage, and writes in the still picture field SIA in 2nd VRAM310. The image data memorized by 1st VRAM670 are read by the superimposition control circuit 420, and the video signal is supplied to a color CRT 701. Therefore, the still picture written in 1st VRAM310 in step S1 will be displayed on a color CRT 701.
[0064] At step S2, a user chooses one person from nine professional golfers displayed as a still picture. At step S3, the image transfer controller 680 reads the animation image data in which a golfer's selected swing jazz is shown from CD-ROM equipment 682, and they are transmitted to the animation field MIA in 2nd VRAM310. Then, as shown in drawing 7 (B), the animation of a golfer's swing jazz is written in in the animation field MIA in 2nd VRAM310.
[0065] As shown in drawing 7 (C), the alphabetic character "the golf classroom" and "A pro's form" which are displayed in a window, and the color key data KY in which the field which superimposes the image in 2nd VRAM310 is shown are written in the window memory area 632 of main memory 630. The image data of the window memory area 632 are transmitted to 1st VRAM670 by CPU620. In addition, when two or more windows are opened on the screen, two or more window memory areas are secured in main memory 630. And the image data in each window memory area are transmitted to 1st VRAM670 by CPU620. And by the video controller 660, the image data stored in 1st VRAM670 are read as a video

signal LSPC, and are supplied to the image processing circuit 800. Therefore, the video signal LSPC containing the color key data KY will be supplied to the image processing circuit 800.
[0066] The signal level of the video signal LSPC corresponding to the color key data KY turns into level more than the reference voltage Vr shown in drawing 2 . Consequently, in the field (superimposition field) in which the color key data KY were set up, the comparison signal COMP compared from the electrical-potential-difference comparator circuit 540 serves as L level, and the video signal LSDA read from 2nd VRAM310 is chosen by the video switch 510, and is supplied to a color CRT 701. On the other hand, in the field in which the color key data KY are not set up, by the video controller 660, the video signal LSPC read from 1st VRAM670 is chosen, and it is displayed on a color CRT 701. If it summarizes, in the superimposition field in which the color key data KY are set up, the image read from 2nd VRAM310 will be displayed, and the image read from 1st VRAM670 will be displayed in the field in which the color key data KY are not set up.
[0067] Drawing 9 is the explanatory view showing the location and size of an image in the 1st example. Drawing 9 (A) shows the size SX of an animation [a dot], and SY [Rhine]. Drawing 9 (B) shows the still picture field SIA and the animation field MIA in 2nd VRAM310. The sizes of a field including the still picture field SIA and the animation field MIA are SXL [a pixel] and SLY [Rhine]. Drawing 9 (C) shows the color key data area in the window memory area 632 (superimposition field). if the starting address (offset address) of the window memory area 632 is set to (X0 and Y0) and the starting address (address of an upper left point) of the color key data area of a still picture is set to (SX0 and SY0) — the difference — the addresses (SX0-X0 and SY0-Y0) are (DH, DY). Drawing 9 (D) shows a screen display in a color CRT 701. The sizes of the animation field MIA in Window W are MH [a pixel] and MV [Rhine], and the sizes of a field including the still picture field SIA and the animation field MIA are MHL [a pixel] and MVL [Rhine].
[0068] The level display scale factor KH and the perpendicular display scale factor KV of an animation of drawing 9 (D) on the basis of the animation of drawing 9 (A) are given by the degree type.
KH=MH/SX — (1a)
KV=MV/SY — (1b)
[0069] Moreover, the address (SX0 and SY0) of the display starting position in Window W is given by the degree type.
SX0 =X0+DH — (2a)
SY0 =Y0+DV — (2b)
[0070] The display sizes MHL and MVL of a field including the still picture field SIA and the animation field MIA on the screen of a color CRT 701 are given by the degree type.
MHL=SXLxKH — (3a)
MVL=SYLxKV — (3b)
[0071] As explained in drawing 6 , the level display scale factor KH of an image is the dividing value N425 of the PLL circuit in the horizontal read-out dot clock generator 425 (drawing 3). It can adjust by adjusting a value. Moreover, the perpendicular scale factor KV of an image is the dividing value N430 of the PLL circuit in the perpendicular read-out Rhine clock generation machine 430. It can adjust by adjusting a value. Specifically, they are these dividing values N425 and N430. A value is given by the degree type.
N425 =NH0/KH — (4a)
N430 =NV0/kV — (4b) NH0 is a dividing value in case the level display scale factor KH is set to 1 here, and NV0 is a dividing value in case the perpendicular display scale factor KV is set to 1.
[0072] Thus, at this example, they are the dividing value N425 of a PLL circuit, and N430. By adjusting, the scaling of the still picture and animation in Window W can be carried out for the same scale factor as coincidence. In addition, the level display scale factor KH and the perpendicular display scale factor KV can be set as a value different, respectively.
[0073] In addition, in case the display scale factors KH and KV are changed, CPU620 carries out the scaling of the color key data area in the window memory area 632 according to these display scale

factors KH and KV. Since there is quite little amount of data of the window memory area 632 compared with the amount of data in VRAM, it can perform the scaling of a color key data area at a high speed by CPU620.

[0074] D. The contents of the image processing in the 2nd example : drawing 10 is the explanatory view showing the contents of processing of the 2nd example of this invention, and drawing 11 is a flow chart which shows the procedure. In addition, processing of drawing 11 is also performed when CPU620 performs the application program stored in main memory 630.

[0075] In the 2nd example, the TV phone system between the computer systems connected to the network is realized. What is shown in drawing 1 as a computer system can be used.

[0076] At step S11 of drawing 11 , a still picture for CPU620 to choose a message partner is read from a hard disk drive unit 654, and it writes in the still picture field in 2nd VRAM310. Consequently, as shown in drawing 10 (A), nine still pictures for choosing a message partner are arranged and displayed on the left half of a window.

[0077] A user's own animation is expressed to the animation field in the right half of a window as step S12 of drawing 11 . In addition, in the 2nd example, the video camera (not shown) for displaying a user's own animation is connected to the image input terminal 103 (drawing 2).

[0078] If a user chooses one message partner from a still picture in step S13, in step S14, the message partner as whom CPU620 was chosen through the network interface 656 will be called. connection with the other party — completing (step S15) — as shown in drawing 10 (B), the image of the message partner transmitted from a message partner's computer system is displayed on the still picture field in a window (step S16). In addition, a message partner's image is supplied to CPU620 through a network interface 656, and is transmitted to the still picture field in 2nd VRAM310 by CPU620. Since a message partner's image is intermittently supplied through a network interface 656, it is displayed on a color CRT 701 as a semi-continuous still picture (half-animation). In addition, a user's own image is also intermittently transmitted to a message partner's computer system through the network interface 656.

[0079] In this way, during the message (step S17), while a message partner's semi-continuous still picture is displayed on the still picture field in a window, a user's own animation is also shown by the animation field. After a message is completed, a circuit is cut in step S18 and it returns to the condition of drawing 10 (step S18) (A).

[0080] Thus, in the 2nd example, the TV phone using a computer system is easily realizable. Under the present circumstances, in a window, not only a message partner's semi-continuous still picture but a user's own animation can be displayed at coincidence. Moreover, it is also possible to carry out the scaling of the still picture and animation in a window for the same scale factor as coincidence like the 1st example, as shown in drawing 9 .

[0081] In addition, this invention can be carried out in various modes in the range which is not restricted to an above-mentioned example or an above-mentioned operation gestalt, and does not deviate from that summary, for example, the following deformation is also possible for it.

[0082] (1) He was trying to compound the video signal LSMEM read from 2nd VRAM310 in the above-mentioned example to the video signal LSPC read from 1st VRAM670 according to the color key data KY stored in 1st VRAM670. However, it is also possible to give the video signal LSPC read from 2nd VRAM310 to a color CRT 701, without compounding with other video signals. In this case, it is also possible to omit 1st VRAM670. Moreover, VRAM310 will have a viewing area in a color CRT 701, and the room corresponding to 1 to 1, and VRAM will be used as a frame memory.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the configuration of the computer system as one example of this invention.
[Drawing 2] The block diagram showing the internal configuration of the image processing circuit 800.
[Drawing 3] The detailed block circuit diagram of the superimposition control circuit 420 and its circumference circuit.
[Drawing 4] The explanatory view showing the I/O circuit of Horizontal Synchronizing signal HSPC in the superimposition control circuit 420, and Vertical Synchronizing signal VSPC.
[Drawing 5] The block diagram showing the configuration of the PLL circuit 63.
[Drawing 6] The explanatory view showing the function of the set point of each circuit in the superimposition control circuit 420.
[Drawing 7] The explanatory view showing the contents of processing in the 1st example of this invention.
[Drawing 8] The flow chart which shows the procedure in the 1st example of this invention.
[Drawing 9] The explanatory view showing the location and size of an image in the 1st example.
[Drawing 10] The explanatory view showing the contents of processing in the 2nd example.
[Drawing 11] The flow chart which shows the procedure in the 2nd example of this invention.
[Drawing 12] The explanatory view showing the condition that the still picture and the animation were displayed by coincidence in one window of a display device.
[Description of Notations]
61 62 — Buffer
62 61 — Buffer
63 — PLL circuit
71 — Phase comparator
72 — Low pass filter
73 — Voltage controlled oscillator (VCO)
74 — N counting-down circuit
101 — Voice input terminal
102 — Voice output terminal
103 — Image input terminal
110 — Sound signal selection circuitry
120 — Sound-volume control circuit
130 — Video-signal selection circuitry
140 — Video-signal decoder
210 — A-D converter
220 — Digitization control circuit
310 — Video RAM (1st image memory)
320 — Image data selection circuitry

330 — Image memory control signal selection circuitry
340 — Write control circuit
350 — Read-out control circuit
360 — FIFO memory
370 — FIFO read-out control circuit
410 — DA converter
420 — Superimposition control circuit
421 — Level criteria read-out dot clock generator
422 — Horizontal read-out initiation counter
424 — Count counter of horizontal read-out
425 — Horizontal read-out dot clock generator
426 — Perpendicular read-out offset counter
427 — The number counter of perpendicular blankings
428 — Perpendicular read-out initiation counter
429 — Count counter of perpendicular read-out
430 — Perpendicular read-out Rhine clock generation machine
431 — AND circuit
432 — OR circuit
433 — NOR circuit
434 — Tri-state circuit
435 — Tri-state circuit
451 — AND circuit
490,491 — Synchronizing signal terminal
506 — Chrominance-signal input terminal
507,508 — Synchronous terminal
510 — Video switch
540 — Electrical-potential-difference comparator circuit
610 — Bus
620 — CPU (processor)
630 — Main memory
632 — Window memory area
640 — Circumference controller
642 — Keyboard
644 — Mouse
650 — Compound I/O Port
652 — Floppy disk drive unit
654 — Hard disk drive unit
656 — Network interface
660 — Video controller
670 — Video RAM (1st image memory)
680 — Image transfer controller
682 — CD-ROM equipment
701 — Color CRT
710 — Television tuner
711 — TV antenna
800 — Image processing circuit (image processing section)

[Translation done.]